



DRV5013-Q1 Automotive Digital-Latch Hall Effect Sensor

1 Features

- Digital Bipolar-Latch Hall Sensor
- AEC-Q100 Qualified for Automotive Applications
 - Grade 1: $T_A = -40$ to 125°C (Q, See [Figure 22](#))
 - Grade 0: $T_A = -40$ to 150°C (E, See [Figure 22](#))
- Superior Temperature Stability
 - $B_{OP} \pm 10\%$ Over Temperature
- High Sensitivity Options (B_{OP} and B_{RP})
 - $+2.7 / -2.7$ mT (AD, see [Figure 22](#))
 - $+6 / -6$ mT (AG, see [Figure 22](#))
 - $+12 / -12$ mT (BC, see [Figure 22](#))
- Supports a Wide Voltage Range
 - 2.7 to 38 V
 - No External Regulator Required
- Open-Drain Output (30-mA Sink)
- Fast 35- μs Power-On Time
- Small Package and Footprint
 - Surface Mount 3-Pin SOT-23 (DBZ)
 - 2.92 mm \times 2.37 mm
 - Through-Hole 3-Pin SIP (LPG)
 - 4.00 mm \times 3.15 mm
- **Protection Features**
 - Reverse Supply Protection (up to -22 V)
 - Supports up to 40-V Load Dump
 - Output Short-Circuit Protection
 - Output Current Limitation
 - OUT Short to Battery Protection

2 Applications

- Power Tools
- Flow Meters
- Valve and Solenoid Status
- Brushless DC Motors
- Proximity Sensing
- Tachometers

3 Description

The DRV5013-Q1 device is a chopper-stabilized Hall Effect Sensor that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

The magnetic field is indicated via a digital bipolar latch output. The IC has an open drain output stage with 30-mA current sink capability. A wide operating voltage range from 2.7 to 38 V with reverse polarity protection up to -22 V makes the device suitable for a wide range of automotive applications.

Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or over current.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5013-Q1	SOT-23 (3)	2.92 \times 2.37 mm
	SIP (3)	4.00 \times 3.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Output State

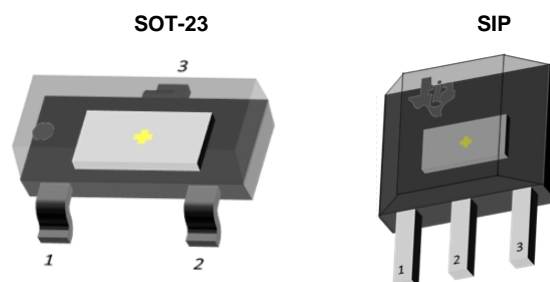
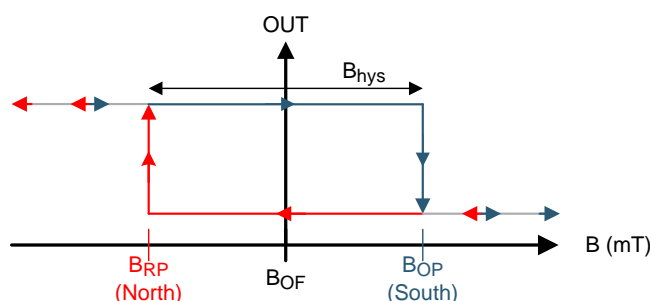


Table of Contents

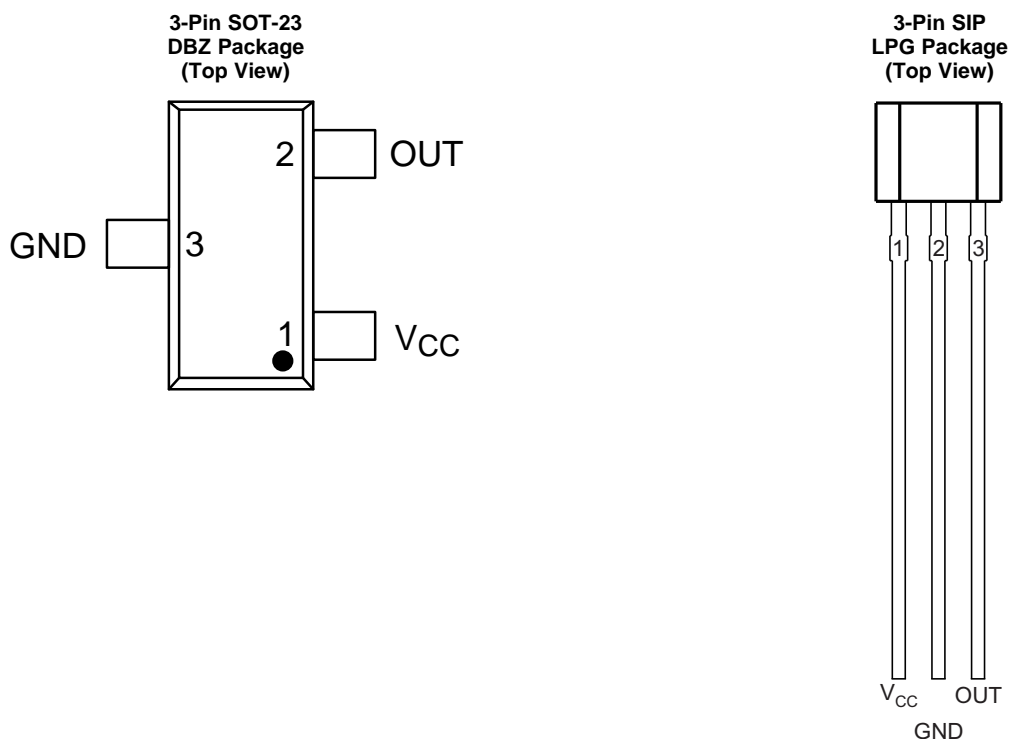
1 Features	1	8 Detailed Description	8
2 Applications	1	8.1 Overview	8
3 Description	1	8.2 Functional Block Diagram	8
4 Output State	1	8.3 Feature Description	9
5 Revision History	2	8.4 Device Functional Modes	14
6 Pin Configuration and Functions	3	9 Application and Implementation	15
7 Specifications	4	9.1 Application Information	15
7.1 Absolute Maximum Ratings	4	9.2 Typical Application	15
7.2 ESD Ratings	4	10 Power Supply Recommendations	17
7.3 Recommended Operating Conditions	4	11 Device and Documentation Support	18
7.4 Thermal Information	4	11.1 Device Support	18
7.5 Electrical Characteristics	5	11.2 Trademarks	19
7.6 Switching Characteristics	5	11.3 Electrostatic Discharge Caution	19
7.7 Magnetic Characteristics	5	11.4 Glossary	19
7.8 Typical Characteristics	6	12 Mechanical, Packaging, and Orderable Information	19

5 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

6 Pin Configuration and Functions

For additional configuration information, see [Device Markings](#) and [Mechanical, Packaging, and Orderable Information](#).



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground terminal
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V _{CC}	1	1	PWR	2.7 to 38 V power supply. Bypass this terminal to the GND terminal with a 0.01-μF (minimum) ceramic capacitor rated for V _{CC} .

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Power supply voltage	V _{CC}	–22 ⁽²⁾	40	V
	Voltage ramp rate (V _{CC}), V _{CC} < 5 V	Unlimited		V/μs
	Voltage ramp rate (V _{CC}), V _{CC} > 5 V	0	2	
Output terminal voltage	OUT	–0.5	40	V
Output terminal reverse current during reverse supply condition	OUT	0	100	mA
Operating junction temperature, T _J	Q, see Figure 22	–40	150 ⁽³⁾	°C
	E, see Figure 22	–40	175 ⁽⁴⁾	
T _{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Ensured by design. Only tested to –20 V.

(3) Tested in production to T_A = 125°C.

(4) Tested in production to T_A = 150°C.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Power supply voltage	2.7	38	V
V _O	Output terminal voltage (OUT)	0	38	V
I _{SINK}	Output terminal current sink (OUT) ⁽¹⁾	0	30	mA
T _A	Operating ambient temperature	Q, see Figure 22	–40	°C
		E, see Figure 22	125	
			–40	150

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV5013-Q1		UNIT
		DBZ	LPG	
		(3 PINS)	(3 PINS)	
R _{θJA}	Junction-to-ambient thermal resistance	333.2	180	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	99.9	98.6	
R _{θJB}	Junction-to-board thermal resistance	66.9	154.9	
ψ _{JT}	Junction-to-top characterization parameter	4.9	40	
ψ _{JB}	Junction-to-board characterization parameter	65.2	154.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V _{CC})						
V _{CC}	V _{CC} operating voltage		2.7		38	V
I _{CC}	Operating supply current	V _{CC} = 2.7 to 38 V, T _A = 25°C		2.7		mA
		V _{CC} = 2.7 to 38 V, T _A = T _{A, MAX} ⁽¹⁾		3	3.5	
t _{on}	Power-on time			35	50	μs
OPEN DRAIN OUTPUT (OUT)						
r _{DS(on)}	FET on-resistance	V _{CC} = 3.3 V, I _O = 10 mA, T _A = 25°C		22		Ω
		V _{CC} = 3.3 V, I _O = 10 mA, T _A = 125°C		36	50	
I _{lkg(off)}	Off-state leakage current	Output Hi-Z			1	μA
PROTECTION CIRCUITS						
V _{CCR}	Reverse supply voltage		−22			V
I _{OCP}	Overcurrent protection level	OUT shorted V _{CC}	15	30	45	mA

(1) T_{A, MAX} is 125°C for Q Grade 1 devices and 150°C for E Grade 0 devices (see Figure 22)

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t _d	Output delay time	B = B _{RP} – 10 mT to B _{OP} + 10 mT in 1 μs		13	25	μs
t _r	Output rise time (10% to 90%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V		200		ns
t _f	Output fall time (90% to 10%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V		31		ns

7.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT ⁽¹⁾
f _{BW}	Bandwidth ⁽²⁾	20			kHz
DRV5013AD: +2.7 / –2.7 mT					
B _{OP}	Operate point; see Figure 12	+1	+2.7	+5	mT
B _{RP}	Release point; see Figure 12	–5	–2.7	–1	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})		5.4		mT
B _O	Magnetic offset; B _O = (B _{OP} + B _{RP}) / 2	–1.5	0	+1.5	mT
DRV5013AG: +6 / –6 mT					
B _{OP}	Operate point; see Figure 12	+3	+6	+9	mT
B _{RP}	Release point; see Figure 12	–9	–6	–3	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})		12		mT
B _O	Magnetic offset; B _O = (B _{OP} + B _{RP}) / 2	–1.5	0	+1.5	mT
DRV5013BC: +12 / –12 mT					
B _{OP}	Operate point; see Figure 12	+6	+12	+18	mT
B _{RP}	Release point; see Figure 12	–18	–12	–6	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})		24		mT
B _O	Magnetic offset; B _O = (B _{OP} + B _{RP}) / 2	–1.5	0	+1.5	mT

(1) 1 mT = 10 Gauss

(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.

7.8 Typical Characteristics

$T_A > 125^\circ\text{C}$ data is valid for Grade 0 devices only (E, see Figure 22)

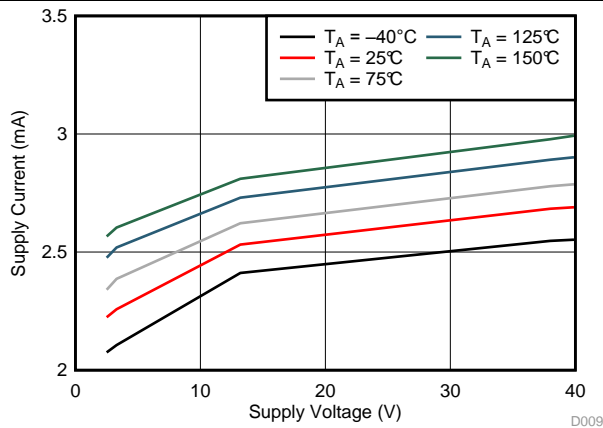


Figure 1. I_{CC} vs V_{CC}

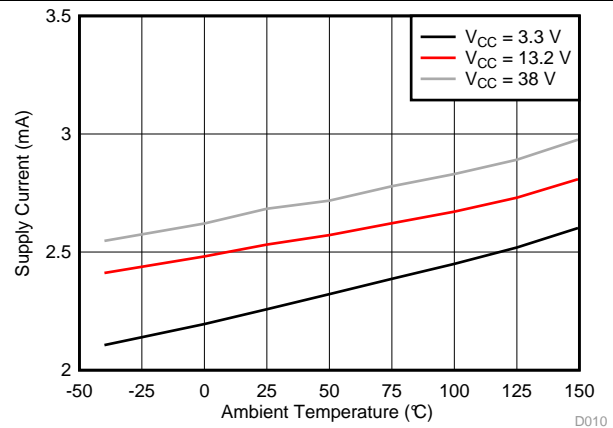


Figure 2. I_{CC} vs Temperature

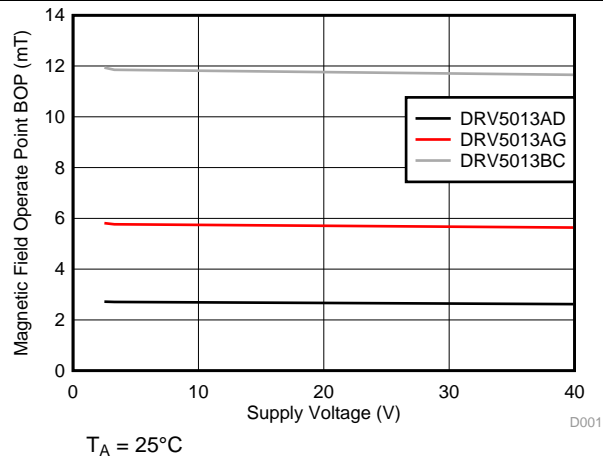


Figure 3. B_{OP} vs V_{CC}

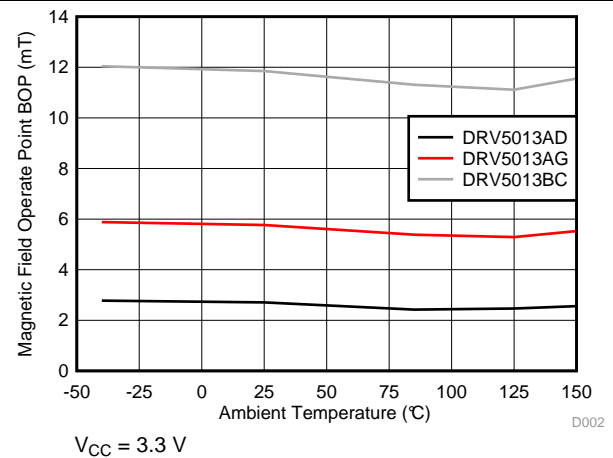


Figure 4. B_{OP} vs Temperature

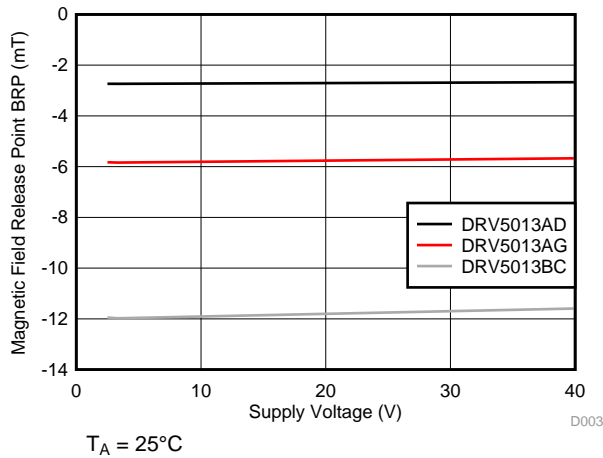


Figure 5. B_{RP} vs V_{CC}

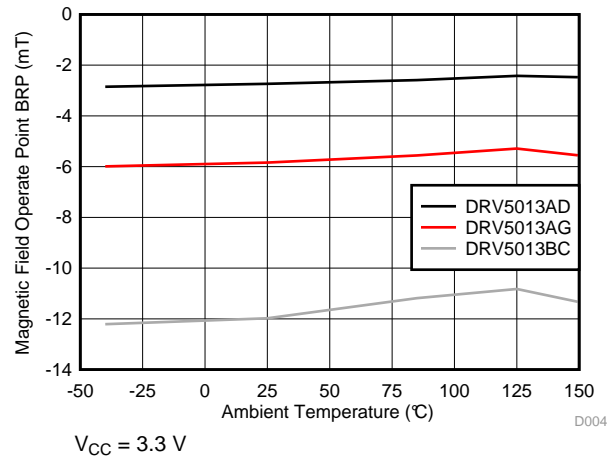


Figure 6. B_{RP} vs Temperature

Typical Characteristics (continued)

$T_A > 125^\circ\text{C}$ data is valid for Grade 0 devices only (E, see [Figure 22](#))

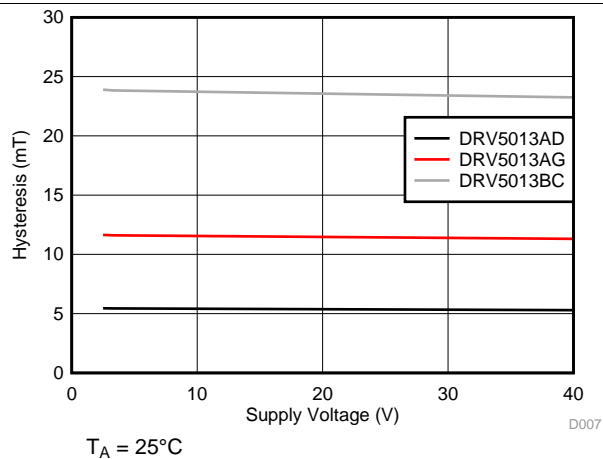


Figure 7. Hysteresis vs V_{CC}

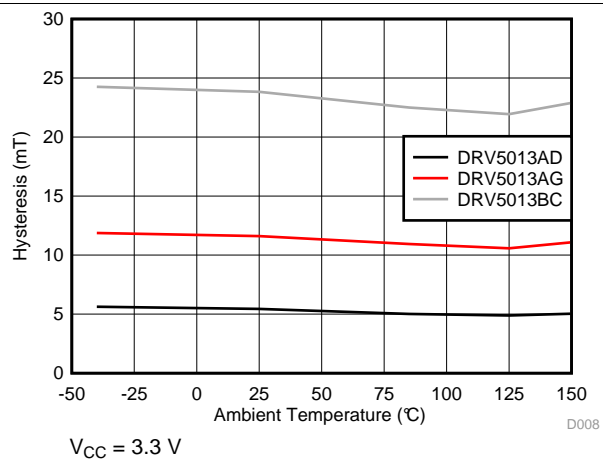


Figure 8. Hysteresis vs Temperature

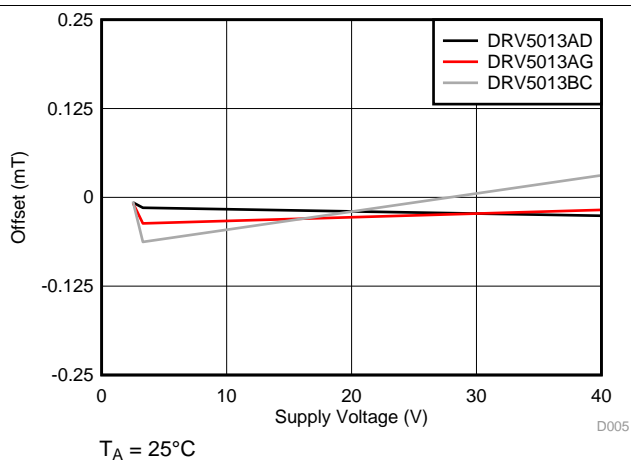


Figure 9. Offset vs V_{CC}

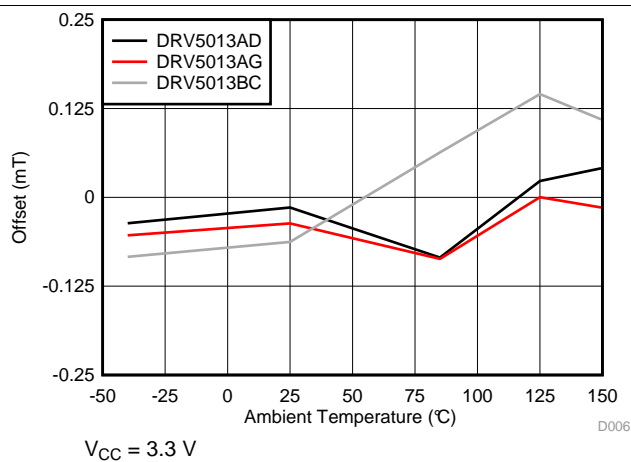


Figure 10. Offset vs Temperature

8 Detailed Description

8.1 Overview

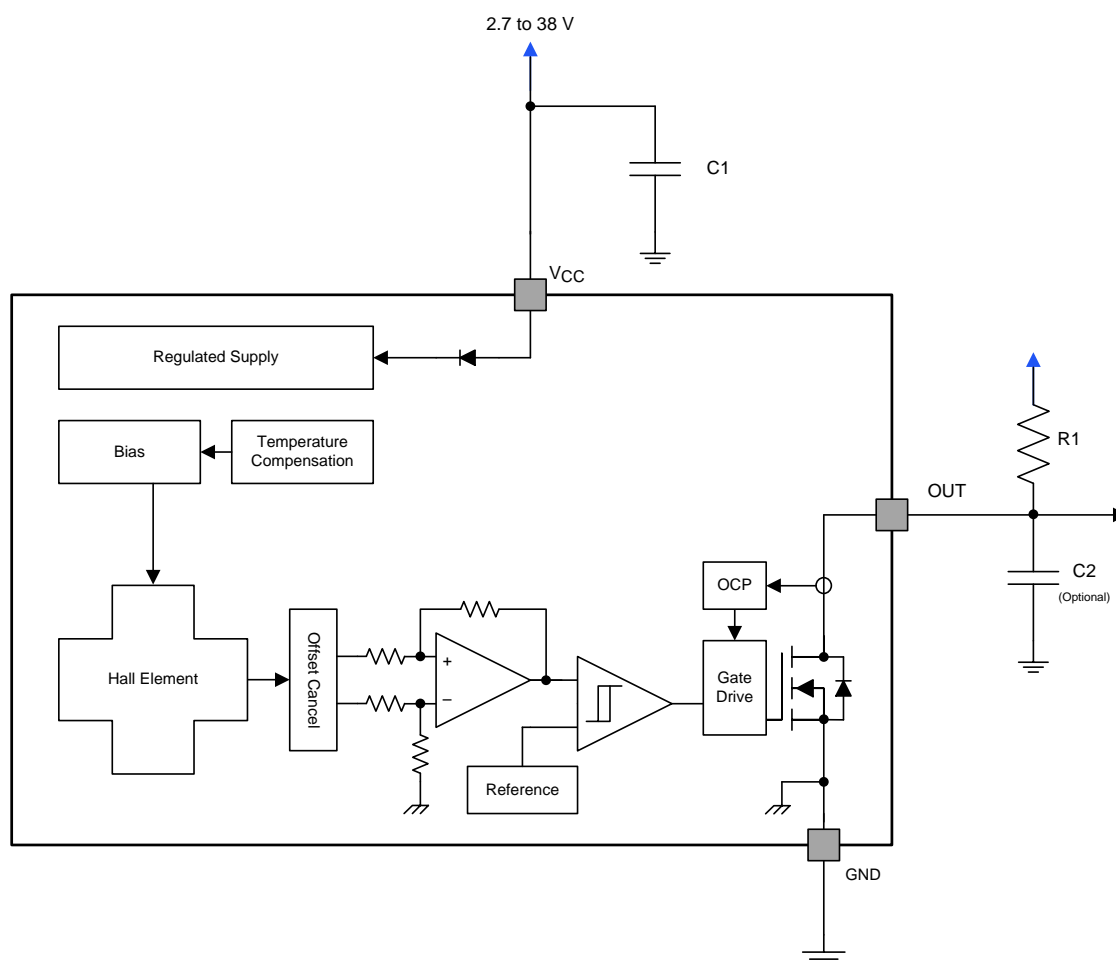
The DRV5013-Q1 device is a chopper-stabilized Hall sensor with a digital latched output for magnetic sensing applications. The DRV5013-Q1 device can be powered with a supply voltage between 2.7 and 38 V, and continuously survives continuous –22-V reverse-battery conditions. The DRV5013-Q1 device does not operate when –22 to 2.4 V is applied to the V_{CC} terminal (with respect to the GND terminal). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a **south pole** near the marked side of the package is a positive magnetic field. A **north pole** near the marked side of the package is a negative magnetic field.

The output state is dependent on the magnetic field perpendicular to the package. A **south pole** near the marked side of the package causes the output to pull low (operate point, B_{OP}), and a **north pole** near the marked side of the package causes the output to release (release point, B_{RP}). Hysteresis is included in between the operate point and the release point therefore magnetic-field noise does not accidentally trip the output.

An external pullup resistor is required on the OUT terminal. The OUT terminal can be pulled up to V_{CC} , or to a different voltage supply. This allows for easier interfacing with controller circuits.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Field Direction Definition

A positive magnetic field is defined as a **south pole** near the marked side of the package as shown in [Figure 11](#).

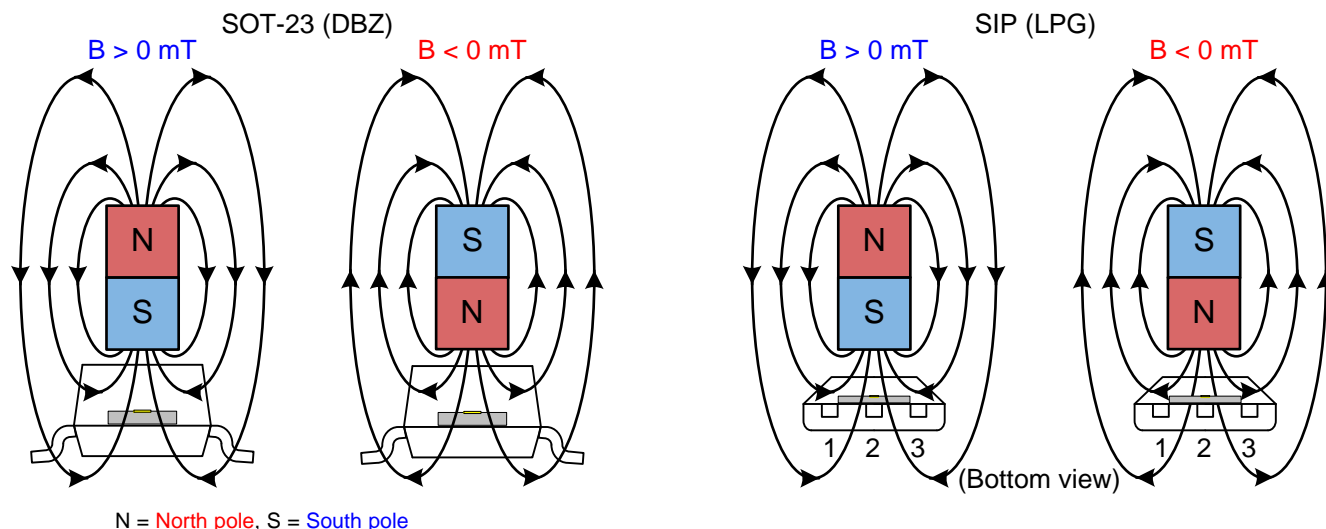


Figure 11. Field Direction Definition

8.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP} , then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP} , then the output is pulled low. If the field strength is less than B_{RP} , then the output is released.

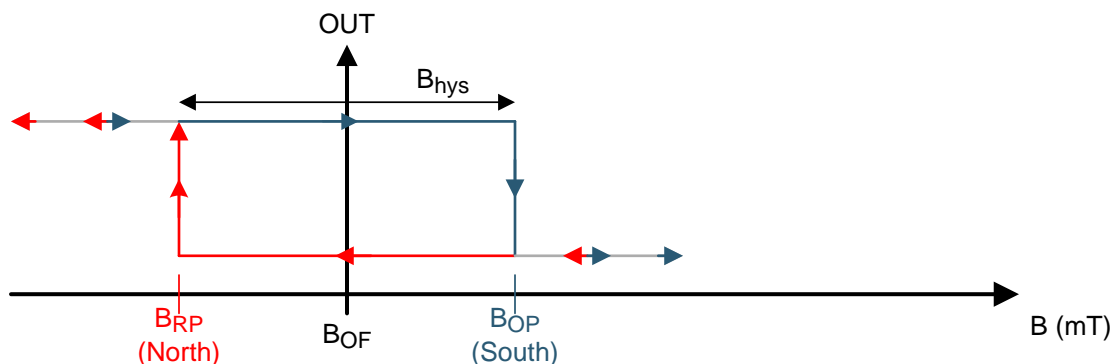


Figure 12. DRV5013-Q1— $B_{OP} > 0$

Feature Description (continued)

8.3.3 Power-On Time

After applying V_{CC} to the DRV5013-Q1 device, t_{on} must elapse before the OUT terminal is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on} . This pulse can allow the host processor to determine when the DRV5013-Q1 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field $B > B_{OP}$ and $B < B_{RP}$.

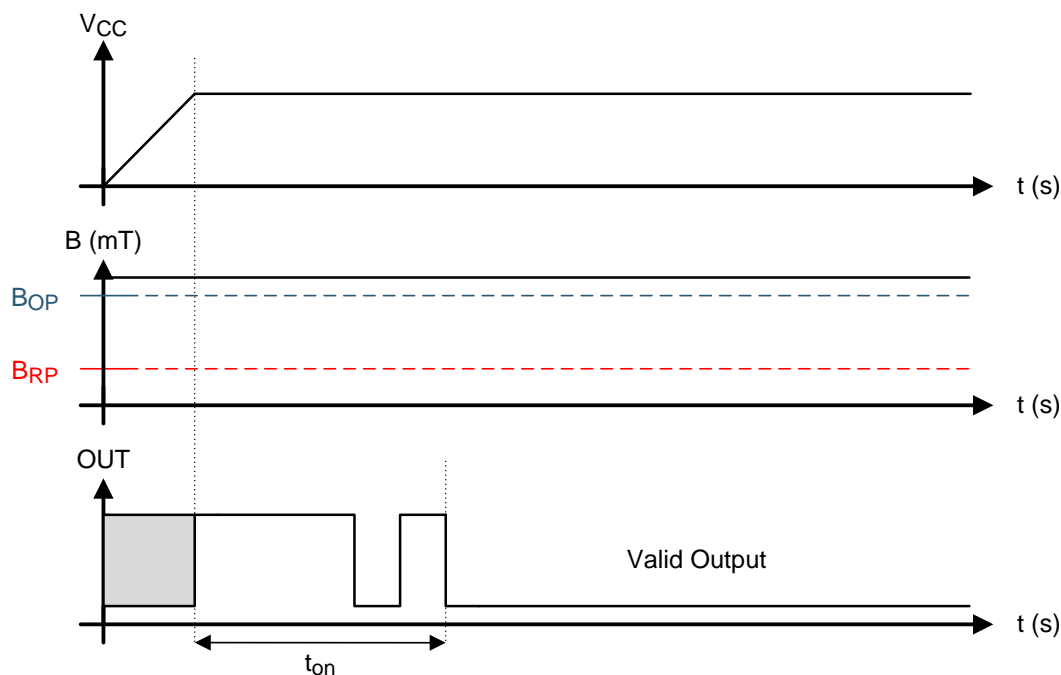


Figure 13. Case 1: Power On When $B > B_{OP}$

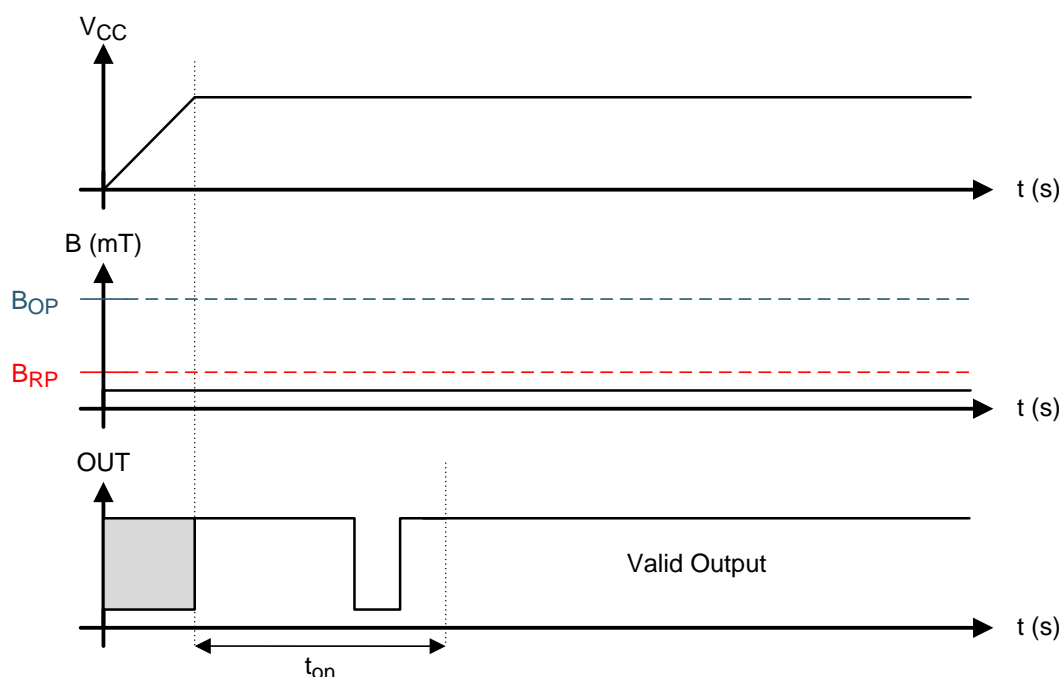


Figure 14. Case 2: Power On When $B < B_{RP}$

Feature Description (continued)

If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on} , a pulse is given on the OUT terminal to indicate that t_{on} has elapsed. After t_{on} , if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

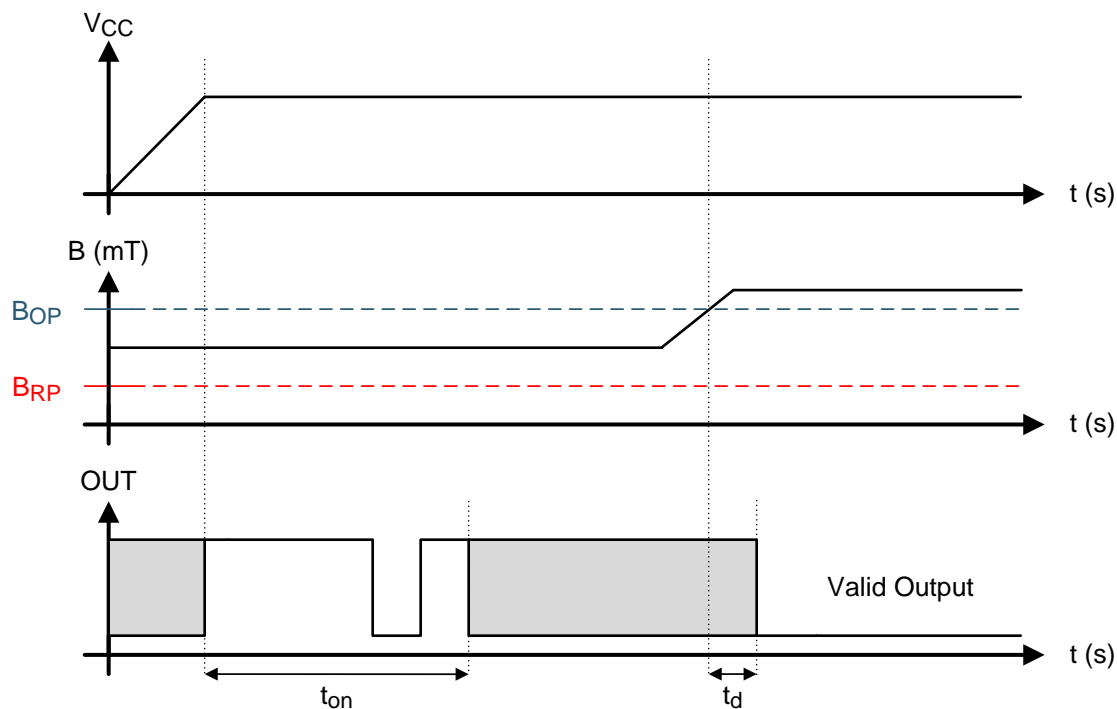


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

Feature Description (continued)

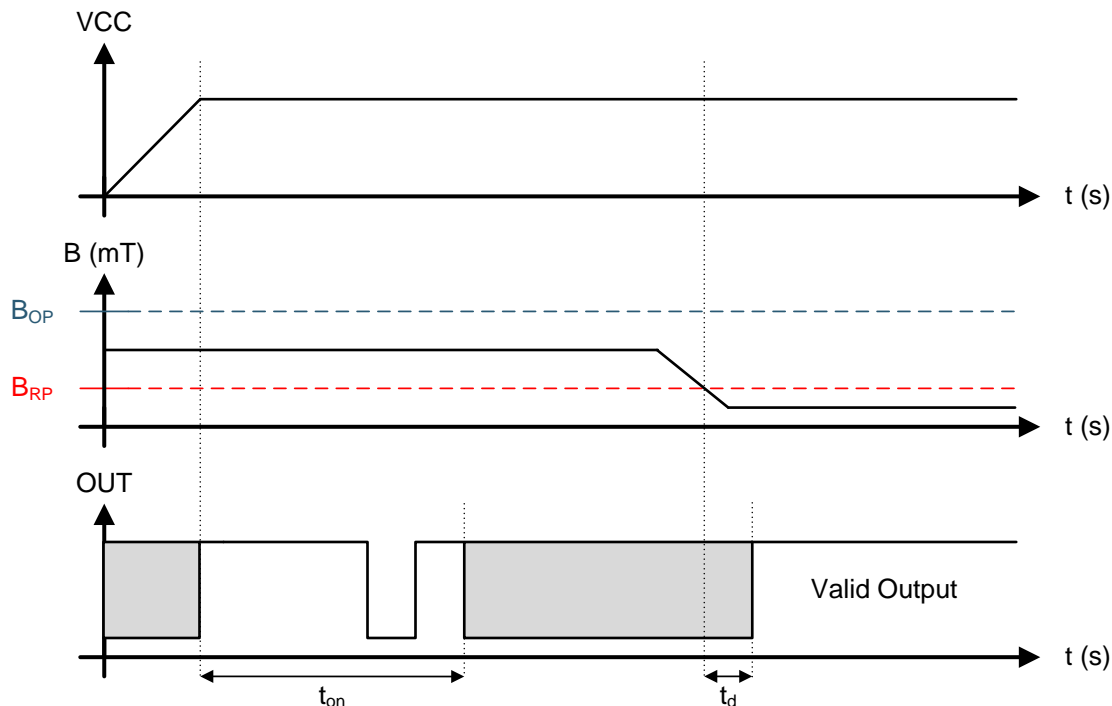


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

8.3.4 Output Stage

The DRV5013-Q1 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using [Equation 1](#).

$$\frac{V_{ref \text{ max}}}{30 \text{ mA}} \leq R1 \leq \frac{V_{ref \text{ min}}}{100 \mu\text{A}} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of $R1 > 500 \Omega$ to ensure the output driver can pull the OUT terminal close to GND.

NOTE

V_{ref} is not restricted to V_{CC} . The allowable voltage range of this terminal is specified in the [Absolute Maximum Ratings](#).

Feature Description (continued)

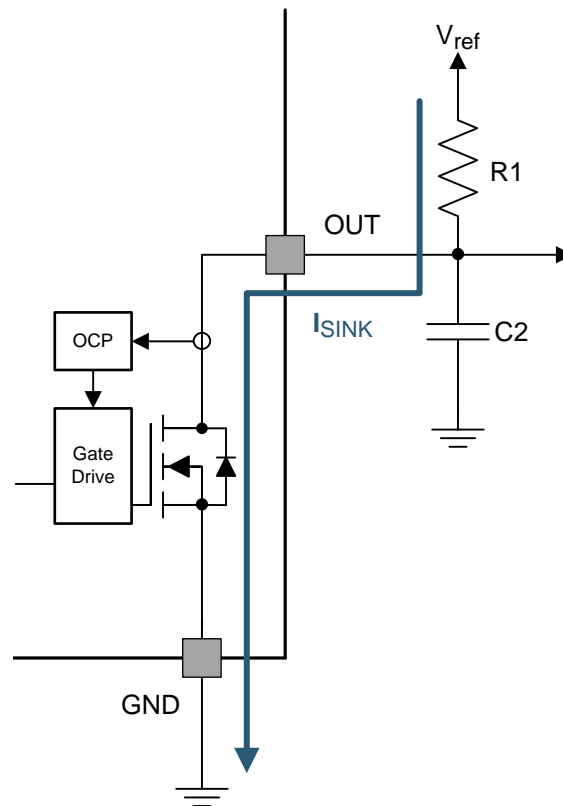


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in [Equation 2](#).

$$2 \times f_{BW} \text{ (Hz)} < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.

Feature Description (continued)

8.3.5 Protection Circuits

The DRV5013-Q1 device is fully protected against overcurrent and reverse-supply conditions.

8.3.6 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP} . During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

8.3.7 Load Dump Protection

The DRV5013-Q1 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand $V_{CC} = 40$ V. No current-limiting series resistor is required for this protection.

8.3.8 Reverse Supply Protection

The DRV5013-Q1 device is protected in the event that the V_{CC} terminal and the GND terminal are reversed (up to -22 V).

NOTE

In a reverse supply condition, the OUT terminal reverse-current must not exceed the ratings specified in the [Absolute Maximum Ratings](#).

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load dump	$38\text{ V} < V_{CC} < 40\text{ V}$	Operating	Device will operate for a transient duration	$V_{CC} \leq 38\text{ V}$
Reverse supply	$-22\text{ V} < V_{CC} < 0\text{ V}$	Disabled	Device will survive this condition	$V_{CC} \geq 2.7\text{ V}$

8.4 Device Functional Modes

The DRV5013-Q1 device is active only when V_{CC} is between 2.7 and 38 V.

When a reverse supply condition exists, the device is inactive.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV5013-Q1 device is used in magnetic-field sensing applications.

9.2 Typical Application

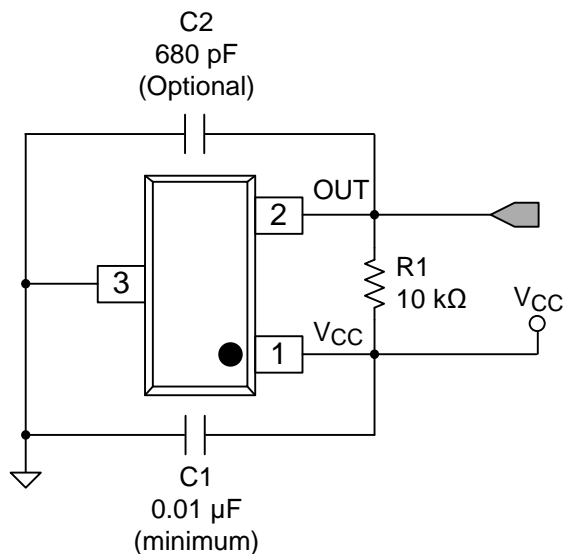


Figure 18. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#) as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

9.2.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-μF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	Optional: Place a ceramic capacitor to GND
R1	OUT	REF ⁽¹⁾	Requires a resistor pullup

(1) REF is not a terminal on the DRV5013-Q1 device, but a REF supply-voltage pullup is required for the OUT terminal; the OUT terminal may be pulled up to V_{CC} .

9.2.2.1 Configuration Example

In a 3.3-V system, $3.2 \text{ V} \leq V_{\text{ref}} \leq 3.4 \text{ V}$. Use [Equation 3](#) to calculate the allowable range for R1.

$$\frac{V_{\text{ref max}}}{30 \text{ mA}} \leq R1 \leq \frac{V_{\text{ref min}}}{100 \mu\text{A}} \quad (3)$$

For this design example, use [Equation 4](#) to calculate the allowable range of R1.

$$\frac{3.4 \text{ V}}{30 \text{ mA}} \leq R1 \leq \frac{3.2 \text{ V}}{100 \mu\text{A}} \quad (4)$$

Therefore:

$$113 \Omega \leq R1 \leq 32 \text{ k}\Omega \quad (5)$$

After finding the allowable range of R1 ([Equation 5](#)), select a value between 500 Ω and 32 k Ω for R1.

Assuming a system bandwidth of 10 kHz, use [Equation 6](#) to calculate the value of C2.

$$2 \times f_{\text{BW}} (\text{Hz}) < \frac{1}{2\pi \times R1 \times C2} \quad (6)$$

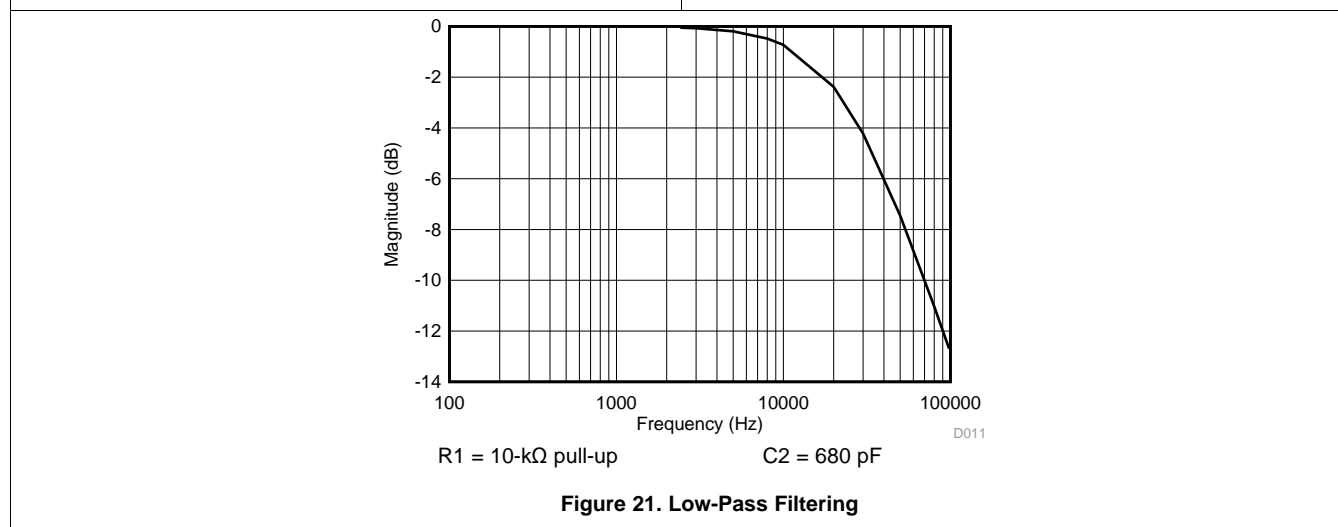
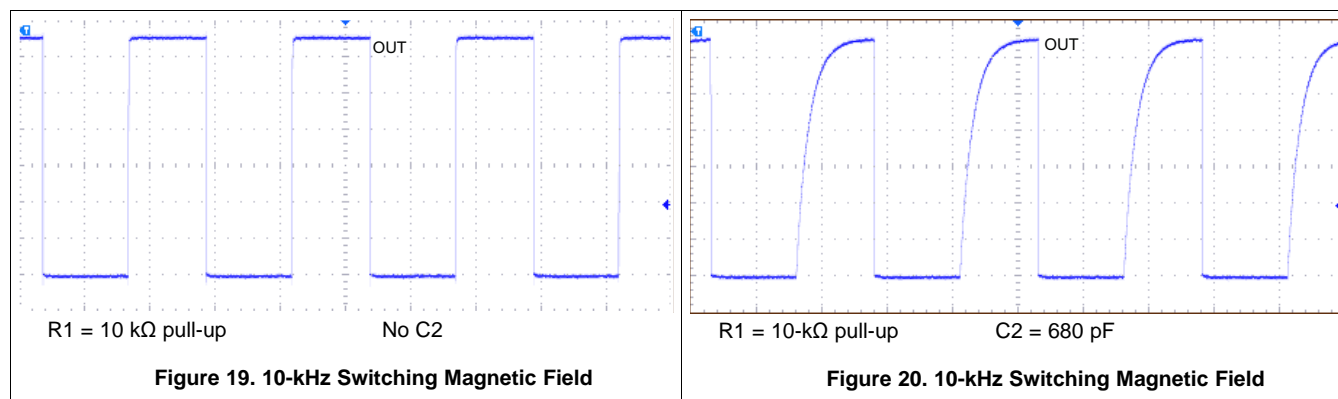
For this design example, use [Equation 7](#) to calculate the value of C2.

$$2 \times 10 \text{ kHz} < \frac{1}{2\pi \times R1 \times C2} \quad (7)$$

An R1 value of 10 k Ω and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

A selection of R1 = 10 k Ω and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

9.2.3 Application Curves



10 Power Supply Recommendations

The DRV5013-Q1 device is designed to operate from an input voltage supply (VM) range between 2.7 and 38 V. A 0.01-μF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5013-Q1 device as possible.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Figure 22 shows a legend for reading the complete device name for and DRV5013-Q1 device.

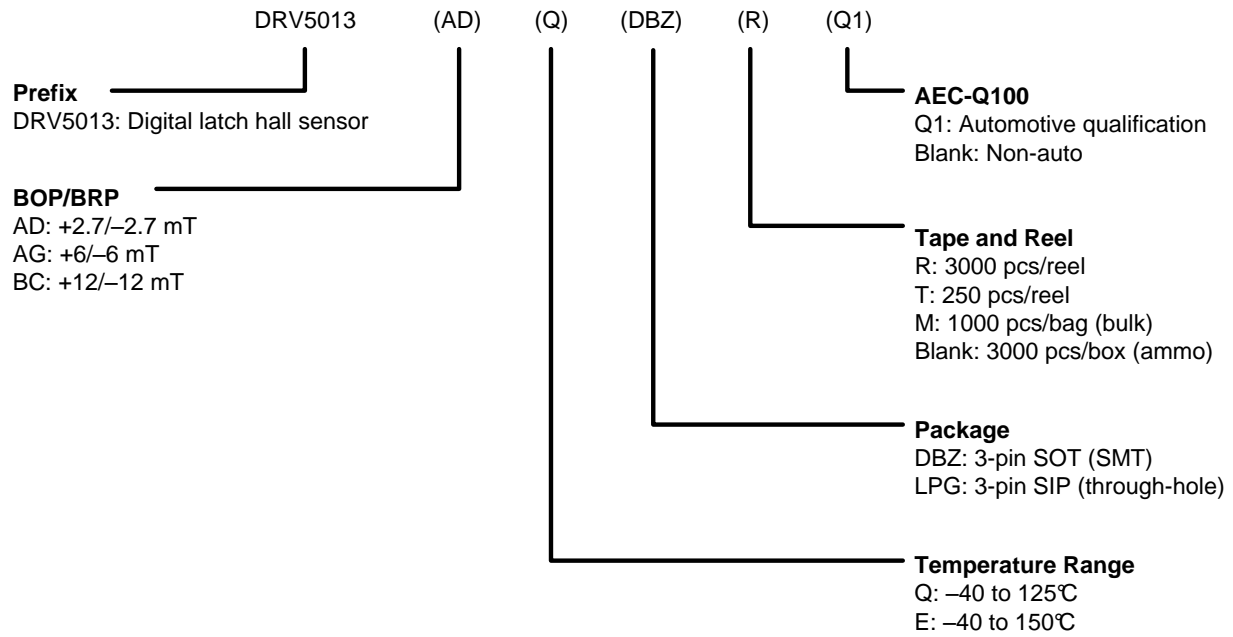


Figure 22. Device Nomenclature

11.1.2 Device Markings

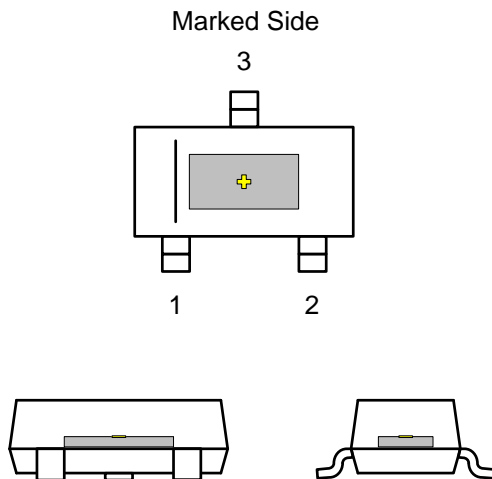


Figure 23. SOT-23 (DBZ) Package

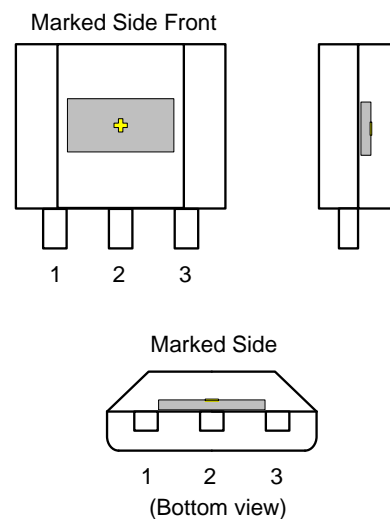


Figure 24. SIP (LPG) Package

✚ indicates the Hall effect sensor (not to scale). The Hall element is located in the center of the package with a tolerance of $\pm 100 \mu\text{m}$. The height of the Hall element from the bottom of the package is $0.7 \text{ mm} \pm 50 \mu\text{m}$ in the DBZ package and $0.987 \text{ mm} \pm 50 \mu\text{m}$ in the LPG package.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5013ADEDDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NJAD	Samples
DRV5013ADEDDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NJAD	Samples
DRV5013ADQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAD	Samples
DRV5013ADQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAD	Samples
DRV5013AGEDDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NJAG	Samples
DRV5013AGEDDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NJAG	Samples
DRV5013AGQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAG	Samples
DRV5013AGQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAG	Samples
DRV5013BCEDDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NJBC	Samples
DRV5013BCEDDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NJBC	Samples
DRV5013BCQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKBC	Samples
DRV5013BCQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKBC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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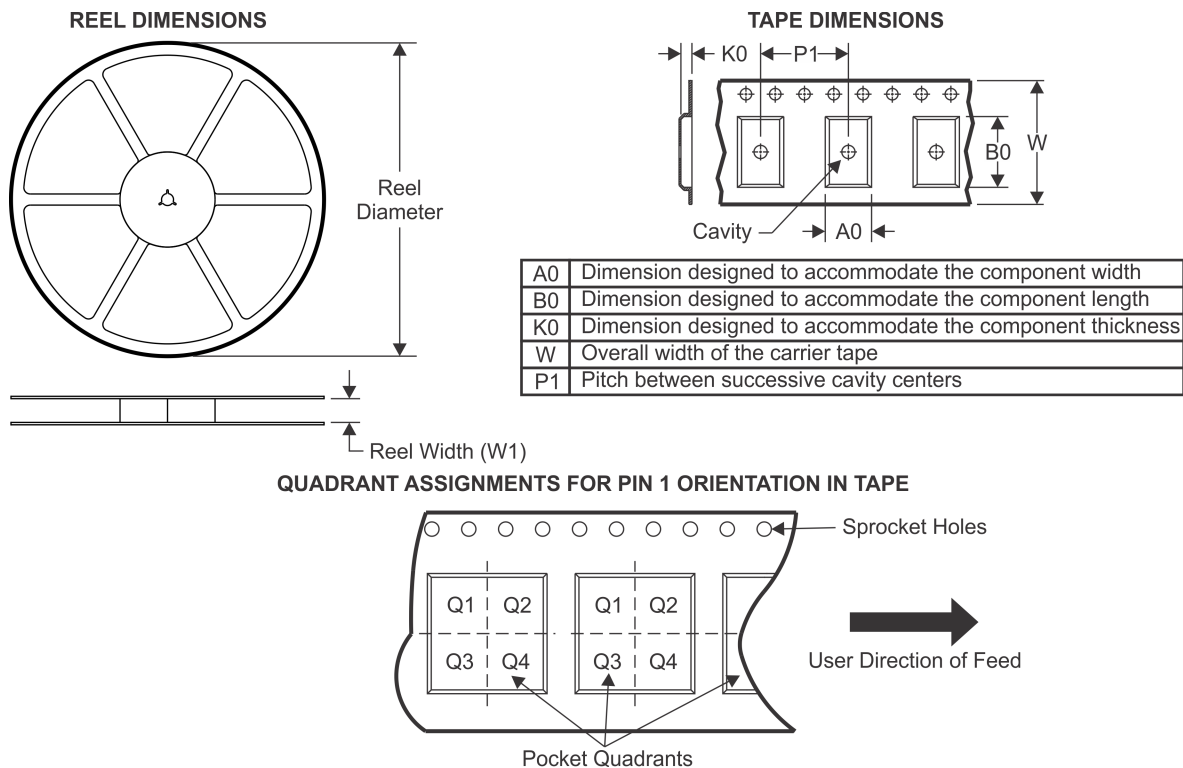
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV5013-Q1 :

- Catalog: [DRV5013](#)

NOTE: Qualified Version Definitions:

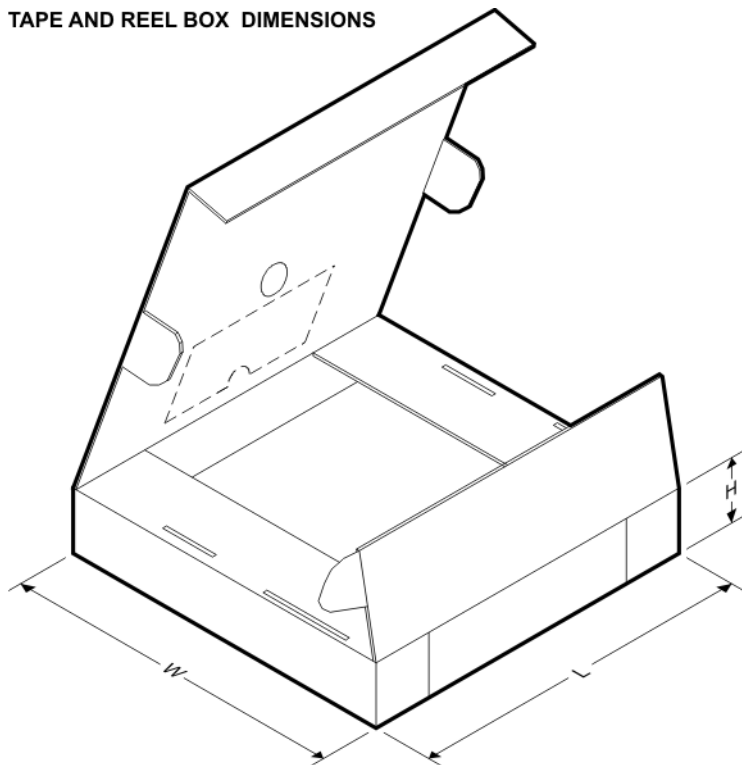
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5013ADEDDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013ADQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013ADQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGEDDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGEDDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCEDDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCEDDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5013ADEDDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013ADQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013ADQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013AGEDDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013AGEDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013AGQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013AGQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013BCEDDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013BCEDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013BCQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013BCQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0



A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Lead dimensions are inclusive of plating.
D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
E. Falls within JEDEC TO-236 variation AB, except minimum foot length.

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